GENERAL

# an asic low power primer analysis techniques and specification

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In the modern era of electronics, the demand for smaller, faster, and more energy efficient devices has never been higher. Whether it's a wearable health monitor, a high performance gaming console, or a next generation data center server, the heart of these systems is a custom Application Specific Integrated Circuit (ASIC). Designing an ASIC that delivers the required performance while consuming minimal power is a complex challenge that blends electrical engineering, computer science, and manufacturing know how. This primer dives deep into the world of low power ASIC design, exploring the essential specifications, the analysis techniques that ensure power goals are met, and the best practices that turn a promising concept into a market ready product.

## Understanding Low Power ASIC Design

### What Is an ASIC?

An ASIC is a silicon chip fabricated to perform a specific set of functions. Unlike general purpose processors, ASICs are optimized for a particular application, allowing designers to squeeze out performance and efficiency that would be impossible on a generic platform. The design flow of an ASIC typically involves:

1. High level specification
2. RTL coding and synthesis
3. Floorplanning and placement
4. Routing and timing closure
5. Power analysis and optimization
6. Verification and tape out

Each of these stages offers opportunities to influence power consumption, but the most critical decisions are usually made early in the design cycle.

### Why Low Power Matters

Power is the single most expensive resource in any electronic system. In battery operated devices, power directly translates to battery life; in large scale data centers, it drives cooling costs and carbon footprint. Moreover, as transistor sizes shrink, leakage currents increase, and dynamic power becomes more volatile. Consequently, low power design is not just a desirable feature—it's a prerequisite for commercial success.

## Key Specifications for Low Power ASICs

### Power Budget

The power budget is the baseline that dictates every subsequent design decision. It is usually expressed in milliwatts (mW) or microwatts (µW) and is derived from system level constraints such as battery capacity, thermal envelope, and performance targets. A typical low power ASIC might aim for a total power consumption below 100 /mW, with dynamic and static components carefully balanced.

### Leakage Current

Leakage current—current that flows even when the transistor is off—has become a dominant power sink in deep sub micron technologies. Specifications often set limits on leakage per unit area or per gate. Designers mitigate leakage through multi threshold CMOS, power gating, and careful transistor sizing.

### Voltage Scaling

Reducing the supply voltage (VDD) is a proven method to cut dynamic power, which scales with the square of the voltage (Pdynamic /= /; ô2 õc" öb'à However, lowering VDD also slows the circuit, so designers create voltage islands that isolate critical paths from low voltage domains.

### Performance Metrics

Key performance metrics include clock frequency, throughput, latency, and data width. Low power design often involves trade offs: a slower clock reduces power but may impact real time requirements. The specification should define acceptable ranges for these metrics to guide optimization.

## Analysis Techniques for Low Power ASICs

### Static Power Analysis

Static power analysis quantifies leakage currents across the entire chip. It involves extracting transistor stacks, gate level models, and employing tools such as Synopsys PrimeTime or Cadence Voltus. The analysis identifies hotspots and guides the placement of sleep transistors or the use of high threshold devices.

### Dynamic Power Analysis

Dynamic power stems from charging and discharging capacitive loads. Tools simulate switching activity (; • using toggling statistics from RTL or gate level simulations. Designers then adjust clock gating, buffer sizing, and interconnect routing to reduce capacitance.

### Power Aware Place and Route

Place and route algorithms can be augmented with power aware heuristics. By clustering low activity blocks together and separating high activity blocks, designers reduce the length of power rails and minimize IR drop. Some EDA suites provide "power aware placement" modes that automatically balance power distribution.

### Floorplanning for Power

Floorplanning is the first physical design step where the layout of blocks is determined. A power centric floorplan places high leakage blocks near power sources, groups dynamic blocks with dedicated voltage islands, and ensures that power rails are short and wide. This step often involves iterative refinement to satisfy both timing and power constraints.

### Power Gating Techniques

Power gating turns off entire blocks or sub circuits by inserting sleep transistors. When a block is idle, the sleep transistor disconnects its supply, eliminating leakage. The design must account for wake up latency and ensure that gating does not violate timing or functional correctness.

### Clock Gating

Clock gating is the most common technique for dynamic power reduction. By disabling the clock to idle registers or logic, the circuit avoids unnecessary switching. The RTL code must include gating logic, and synthesis tools must preserve it.

### Multi Threshold CMOS (MTCMOS)

MTCMOS uses transistors with different threshold voltages (Vth) in the same circuit. Low Vth devices drive speed, while high Vth devices reduce leakage. The design flow must balance area overhead with power savings.

### Voltage Islands

Voltage islands allow different portions of the chip to operate at distinct supply voltages. This technique reduces dynamic power on non critical blocks while maintaining performance on critical paths. The specification should define island boundaries, voltage levels, and inter island communication protocols.

### Power Distribution Network (PDN) Analysis

PDN analysis ensures that voltage regulators, decoupling capacitors, and power rails deliver stable supply voltages under load. Tools model IR drop, capacitance, and inductance to verify that each block receives the required voltage margin. Poor PDN design can cause timing violations and increased dynamic power.

### Simulation and Verification

Power simulation is integrated into functional verification flows. RTL simulators (e.g., ModelSim, VCS) can estimate power by instrumenting toggles, while gate level simulators provide more accurate activity maps. Post layout simulations confirm that the physical implementation meets the power budget.

### Design for Test (DFT) and Power

DFT features such as scan chains and built in self test (BIST) can introduce additional switching activity. Power aware DFT design incorporates test logic into the power analysis flow, ensuring that test patterns do not violate power constraints. Techniques like “low power scan” or “power aware test vector” selection mitigate this issue.

## Tools and Methodologies

### EDA Tools

Modern ASIC design relies on a suite of Electronic Design Automation (EDA) tools:

- Synopsys Design Compiler for RTL synthesis
- Cadence Genus for synthesis and static timing analysis
- Synopsys PrimeTime for static timing and power analysis
- Cadence Voltus for dynamic power estimation
- Mentor Graphics Calibre for physical verification

### Power Estimation Tools

Accurate power estimation requires detailed models. Tools like Synopsys Power Compiler or Cadence Power Compiler generate power models that integrate with the synthesis flow, allowing designers to see power impact of RTL changes in real time.

### Formal Verification

Formal methods prove that a design meets timing, functional, and power constraints. Techniques such as model checking or equivalence checking can verify that power gating logic behaves correctly, preventing subtle bugs that could lead to power spikes.

### Physical Verification

Post layout checks (DRC, LVS, and RC extraction) ensure that the fabricated chip matches the design intent. Power aware physical verification tools check for violations in power grid design, IR drop, and electromigration.

## Best Practices and Checklist

### Early Power Planning

Power planning should begin at the specification stage. Early identification of critical paths, voltage islands, and power budgets saves time and cost later in the design cycle.

### Power Aware RTL Coding

RTL should include explicit power gating and clock gating controls. Using standard cell libraries that support power gating and employing design patterns that minimize switching activity (e.g., avoiding unnecessary register updates) are essential.

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